UNITED STATES PATENT APPLICATION

of

Rudolf J. Hofmeister

and

Lewis Aronson

for

AUTOMATIC SELECTION OF DATA RATE FOR OPTOELECTRONIC DEVICES

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ATTORNEYS AT LAW
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UTAH 84111

AUTOMATIC SELECTION OF DATA RATE FOR OPTOELECTRONIC DEVICES

CROSS-REFERENCE TO RELATED APPLICATIONS

[001]   This application is a continuation-in-part of United States Patent Application Serial No. 10/420,027, *"Transceiver Module and Integrated Circuit With Dual Eye Openers,"* filed April 17, 2003, which claims the benefit of: United States Provisional Patent Application Serial No. 60/410,509, filed September 13, 2002; and, United States Provisional Patent Application Serial No. 60/391,877, filed June 25, 2002. Additionally, this application claims the benefit of United States Provisional Patent Application Serial No. 60/422,806, entitled *"Automatic Selection of Data Rate for Transceivers and Transponders,"* filed on October 30, 2002. Each of the foregoing patent applications is incorporated herein in its respective entirety by this reference.

BACKGROUND OF THE INVENTION

The Field of the Invention

[002]   The present invention relates generally to optoelectronic systems and devices. More specifically, embodiments of the present invention relate to automatic data rate selection in transceivers and transponders.

The Related Technology

[003]   The proliferation and significance of networking technology is well known. Optical transponders and transceivers are used for receiving and transmitting data between electronic hosts such as computers using an optical network. Generally, optical transceivers/transponders are located at the interface of an optical network and

an electronic host. Transceivers and transponders receive optical data signals from the network, convert the optical data signal to an electrical data signal, and pass the electric data signal to the host.

[004]   Likewise, optical transceivers and transponders receive data, in the form of an electrical signal, from the host. The transceiver or transponder converts the electrical signal to an optical data signal, and transmits the optical data signal across an optical network to another host.   Optical transceivers and transponders are commonly implemented in the form of a combination transceiver/transponder module that can be mounted on a motherboard of a host via an interconnect.

[005]   The ever-increasing demand for network bandwidth has resulted in the development of technology that increases the amount of data traveling across a network. Advancements in modulation techniques, coding algorithms and error correction have drastically increased rates of this data type. For example, it was the case at one time that the highest rate that data could travel across a network was at approximately one Gigabit per second ("GB/s"). Subsequently however, data rates of 10GB/s have been achieved in connection with Ethernet and Synchronous Optical Network ("SONET") networks. For instance, the XFP (10 GB/s serial electrical interface) Pluggable Module Multi-Source Agreement ("MSA") is directed to transceivers operating at approximately 10 Gb/s. Further, data rates of 4 Gb/s have been attained in Fibre Channel ("FC") networks.

[006]   As data rates have increased, transceivers and transponders have been designed to be compatible with networks that run at different data rates. For instance, in a Fibre Channel network, it may be desirable to operate at a data rate of about 4, 2, or 1 Gb/s or lower. In a Ethernet or SONET system, the transceiver or transponder may operate at a

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data rate of about 10, 5, or 1 Gb/s or lower. In yet other systems, it may be desirable to select a single operational data rate, or a range of data rates over which the system will operate. As an example of the latter case, it may be necessary to set a transceiver or transponder to operate at one of several data rates close to 10 Gb/s.

[007] Many existing transceivers and transponders have selectable data rates. Conventionally, a transceiver/transponder module with a selectable data rate will include a data rate select pin that allows the transceiver/transponder module to be configured or set to operate at one of several rates. Thus, transceivers and transponders with selectable data rates allow the transceiver or transponder to be configured for use in various types of networks and network configurations.

[008] However, existing transceivers and transponders are problematic in that they typically require a user to manually select the data rate. The requirement for manual selection of the data rate for the transceiver or transponder limits the ability of the transceiver/transponder to respond to system changes. This limitation can cause problems in some situations, such as by preventing certain networks from working together.

[009] A related problem concerns the fact that an I/O connector, such as a pin on the interconnect between the transceiver/transponder and the host board, is required in some instances to facilitate implementation of the data rate selection or change. Oftentimes, the pin arrangement for a transceiver/transponder module is defined by industry standard, so that a desired new feature or component cannot be added to the transceiver/transponder module if adding that feature would require some type of I/O to control the data rate of operation and/or if no I/O connection is available for the transceiver/transponder module under the existing industry standard.

[010] Therefore, what is needed are optoelectronic components, such as transceivers, transponders, and transceiver/transponder modules for example, whose operational data rate can be automatically selected. Moreover, at least some implementations of such optoelectronic components should be self-contained such that automatic data rate selection can be implemented by the optoelectronic component without regard to the configuration of the associated host board.

BRIEF SUMMARY OF AN EXEMPLARY EMBODIMENT
OF THE INVENTION

[011] In one exemplary embodiment of the present invention, a transceiver/transponder module is provided that includes, among other things, signal modification circuitry. The signal modification circuitry is exemplarily implemented as a clock and data recover ("CDR") integrated circuit ("IC"), or CDR IC, and is configured to operate at a variety of different data rates. In one embodiment, the CDR IC includes an input for receiving an input data stream and an input for selecting the operational data rate of the CDR IC. Among other things, the CDR IC is configured to generate a loss of lock ("LOL") signal when the data rate of the input data stream deviates from the selected data rate of the CDR IC by a predetermined margin.

[012] In this regard, this exemplary embodiment of the transceiver/transponder module further includes a controller that monitors the CDR IC for the LOL signal. Upon sensing the LOL signal, the controller automatically adjusts the selectable data rate of the CDR IC until the LOL signal ceases. More particularly, the controller, upon detection of an LOL, automatically begins testing a discrete number of possible data rates. If the LOL signal ceases, the controller sets the CDR IC to operate at the selected rate. If all selectable data rates are attempted and the LOL signal persists, the controller sets the data stream to bypass the CDR IC.

[013] It should be noted that in a system designed to operate at a very wide range of data rates, such as between Ethernet rate of 1.25 Gb/s and the 10 Gigabit Ethernet rate of 10.3125 Gb/s, the retiming function in a serial transceiver may only be needed at the higher data rates where it is being used to compensate for signal degradations which are insignificant at the higher data rates. Thus, a system which recognizes the very low

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rates, by the above process of elimination or otherwise, and ultimately bypasses the retiming function, would be expected to provide totally adequate performance at the much lower data rates. The bypass mode, referred to elsewhere herein, is therefore not a failure mode, but instead a feature of normal operation whereby system operation may be achieved far outside the available data rate range of a given CDR IC.

[014] Among other things then, exemplary embodiments of the invention allow optoelectronic devices such as transceivers and transponders to transmit at more than one data rate without the need for manual adjustment of the data rate of the IC. Moreover, such automatic implementation of data rate changes can be accomplished internally within the optoelectronic device, without the need for devices such as I/O connections. The foregoing, and other, aspects of the present invention will become more fully apparent from the following description and appended claims.

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BRIEF DESCRIPTION OF THE DRAWINGS

[015] In order that the manner in which the above-recited and other aspects of the invention are obtained, a more particular description will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only exemplary embodiments of the invention and are not therefore to be considered limiting of its scope, exemplary embodiments of the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

[016] Figure 1 is a block diagram illustrating aspects of a system that includes a host device configured to communicate with a transceiver/transponder module that enables automatic selection of an operational data rate;

[017] Figure 2 is a block diagram that illustrates further aspects of the transceiver/transponder module of Figure 1;

[018] Figure 3 is a block diagram of an alternative implementation of a transceiver/transponder module that enables automatic selection of an operational data rate; and

[019] Figure 4 is a block diagram of another implementation of a transceiver/transponder module that enables automatic selection of an operational data rate.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[020] Exemplary embodiments of the invention are generally concerned with systems and devices for implementing automatic control of the data rate of rate-selectable optical, electrical, and optoelectronic devices. Embodiments of the invention are compatible with a wide variety of data rates and physical protocols, and can be employed in connection with a range of optical, electronic and optoelectronic systems and devices. In various exemplary embodiments, such optical, electrical, and optoelectronic devices are configured to transmit signals over the network at data rates including, but not limited to, about 1.25 Gb/s, about 2 Gb/s, about 2.5 Gb/s, about 4 Gb/s, and about 10 Gb/s. Exemplary protocols with which embodiments of the invention are compatible include, but are not limited to, Gigabit Ethernet, Fibre Channel, and SONET and 10 Gigabit Ethernet.

[021] Among other things, exemplary embodiments of the invention allow optoelectronic devices such as transceivers and transponders to transmit at a variety of different data rates without the need for manual adjustment of the data rate of the IC. Moreover, such automatic implementation of data rate changes can be accomplished internally within the optoelectronic device, without the need for devices such as I/O connections. Further, exemplary embodiments of the invention enable the automatic selection of data rates in transceivers and transponders using various rate-selectable integrated components. For instance, various embodiments of the present invention automatically select the data rates in transceivers/transponders by adjusting the data rate of a CDR, a MUX/DEMUX, a SERDES, or other component or device.

[022] By way of example, in one exemplary embodiment, the IC includes a clock and data recover ("CDR") IC. Generally, the CDR IC is configured to generate the LOL

signal when the input data stream is out or range. In another exemplary embodiment, a multiplexer/demultimplexer ("MUX/DEMUX") generates the LOL signal. In a further exemplary embodiment, a serializer/deserializer ("SERDES") generates the LOL signal. In some implementations, the MUX/DEMUX and the SERDES includes a CDR that generates the LOL signal.

[023] Additionally, at least some embodiments are configured so that the IC automatically selects a data rate without instruction or input from a controller or external clock. Exemplarily, the IC includes a CDR that generates an LOL signal when the input data stream is out of range of the selected data rate for the IC.

I. General Aspects of an Exemplary Transceiver/Transponder Module

[024] With attention now to Figure 1, details are provided concerning various aspects of an exemplary system 100 that includes a transceiver/transponder module 200 and host device 300 configured and arranged to interact with each other. Generally, such interaction is facilitated through the use of transmission lines 102 and 104 that electronically connect the transceiver/transponder module 200 with the host device 300. It should be noted that while the illustrated implementation refers to a transceiver/transponder module 200, embodiments of the invention are not so limited. Rather, embodiments of the invention may, more generally, be employed with any other optical, electronic, or optoelectronic device in connection with which it would be desirable to implement the functionality disclosed herein.

[025] Among other things, the transceiver/transponder module 200 defines a 'receive' path 202A and a 'transmit' path 202B. Elements of the 'receive' path 202A include a receiver 204 and a signal modifier IC 206. Generally, the receiver 204 is configured

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and arranged to receive an optical data signal from a network, or an optical device, and to convert the received optical data signal into an electrical data signal that is then passed to the signal modifier IC 206.

[026] More particularly, the illustrated exemplary embodiment of the receiver 204 includes a receive optical sub-assembly 204A ("ROSA") that receives the optical data signal from the network or optical device and converts the optical data signal to an electrical data signal. Exemplarily, the ROSA comprises a photodiode, but other suitable optoelectronic devices may be employed as well. The receiver 204 also includes a post-amplifier 204B that, in general, serves to amplify, and/or otherwise condition or process, the electrical data signal received from the ROSA 204A. Exemplarily, the signal modifier IC 206 and postamplifier 204B may be combined into a single IC.

[027] With continuing reference to Figure 1, the transmit path 202B defined by the transceiver/transponder module 200 includes a transmitter 208 coupled to a network and a signal modifier IC 210. Generally, the transmitter 208 is configured and arranged to receive an electrical data signal from a host or other system or device, by way of the signal modifier IC 210, and to convert the received electrical data signal into an optical data signal that is then transmitted onto a network or to an optical device.

[028] More particularly, the illustrated embodiment of the transmitter 208 includes a transmitter optical sub-assembly ("TOSA") 208A that receives, at least indirectly, the electrical data signal from the host 300 or other system or device and converts the electrical data signal to an optical data signal and transmits the optical data signal onto a network or to an optical device. Exemplarily, the TOSA 208A includes a laser diode, but other suitable optoelectronic devices may be employed as well. The transmitter 208

also includes a laser driver 208B that generally serves to control operation of the laser within the TOSA 208A. Such control may extend to, among other things, laser input power, and optical amplitude modulation. The laser within TOSA 208A is also biased to the proper operating current using a dedicated biasing and control circuit that may be contained within, or located outside of, the laser driver 208B.

[029] With continuing attention to Figure 1, further details are provided concerning the signal modifier IC 206 and signal modifier IC 210 employed in connection with the exemplary implementation of the transceiver/transponder module 200. In particular, the signal modifier IC 206 is positioned between the receiver 204 and the host device 300, while the signal modifier IC 210 is positioned between the transmitter 208 and the host device 300. Typically, the signal modifier ICs 206 and 210 serve to modify or condition the data stream. More particularly, signal modifier ICs 206 and 210 may include a CDR that reshapes and retimes a data stream to perform an eye-opening function. Alternatively, signal modifier ICs 206 and 210 may include a MUX/DEMUX, SERDES, or an adaptive equalizer.

[030] Various factors may be considering in reaching a determination as to which components will be included in a particular implementation of signal modifier ICs 206 and 210. Typically, such determinations are made without reference to the need to toggle between two or more different operational data rates. For instance, industry standards require XBI transponder modules to have multiplexers and SERDES so that the signal can be transmitted to the host board in parallel. XFP type transceiver modules, however, transmit to the host board in serial fashion, in which case multiplexers and SERDES are not required to interface with the host.

[031] One aspect of the exemplary signal modifier ICs 206 and 210 is that they operate at a selectable data rate. As described below with reference to specific exemplary embodiments of the present invention, the signal modifier ICs 206 and 210 are configured to generate an LOL signal. In general, the input data stream to the transceiver/transponder module 200 is determined to be 'out of lock' when the data rate of the input data stream is outside the operational data rate range specified in connection with signal modifier ICs 206 and 210.

[032] It should be noted that the data rate adjustment, and other, functionality implemented in connection with exemplary embodiments of the invention may be performed in connection with software, as discussed in further detail elsewhere herein. Alternatively, at least some of such functionality may be specified and implemented through the use of field programmable gate arrays ("FPGA") or similar devices.

II. Aspects of Exemplary CDR Signal Modification Circuitry

[033] Direction attention now to Figure 2, details are provided concerning an exemplary implementation of a transceiver/transponder module 200 that incorporates, among other things, automatic data rate selection capabilities. The illustrated embodiment of the transceiver/transponder module 200 includes a signal modifier IC 212 that includes a transmitter clock and data recover ("Tx CDR") 214A and a receiver clock and data recover ("Rx CDR") 214B, each of which is configured to receive various inputs and generate various outputs. It should be noted that Tx CDR 214A and Rx CDR 214B, and IC 212, and other circuitry of transceivers/transponders may be integrated on a single IC, or configured as discrete components, as suggested by the phantom line in Figure 2.

[034] In general, Tx CDR 214A and Rx CDR 214B perform an eye-opening function for a transmitter input data stream 402 (see below) or a receiver output data stream 504 (see below). Further, the Tx CDR 214A and Rx CDR 214B retime and reshape data pulses. Finally, each of the Tx CDR 214A and Rx CDR 214B may include various sub-circuits for providing data at specific data rates.

[035] With more particular reference now to Figure 2, the Tx CDR 214A is configured to receive a data input 402 from the host 300 (see Figure 1), as well as a reference clock input 404. Generally, the Tx CDR 214A uses the reference clock input 404 to center the frequency used to recover the clock and data from an input data stream. In some implementations, the reference clock input 404 is shared by Tx CDR 214A and Rx CDR 214B, thereby reducing the number of components on IC 212 and reducing the complexity and cost of the transceiver/transponder module 200. In addition to the foregoing, the Tx CDR 214A generates a data output 406 to transmitter 208 (see Figure 1).

[036] With continuing reference to Figure 2, the Rx CDR 214B receives, on the receive path 202A, an input 502 from the receiver 204 (Fig. 1). The Rx CDR 214B also generates a data output 504. As discussed in further detail below, 'data rate select' pins 602 and 604 couple a controller 216 to Tx CDR 214A and Rx CDR 214B, respectively.

[037] More particularly, the respective data rate pins 602 and 604 enable selection of an operational data rate. If the data rate of the input data stream 402 is out of the range of the selected data rate of Tx CDR 214A and Rx CDR 214B, the Tx CDR 214A and/or Rx CDR 214B, as applicable, generates a loss of lock ("LOL") signal. However, if Tx CDR 214A or Rx CDR 214B is locked, no LOL signal is generated for the respective

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CDR. In the exemplary arrangement illustrated in Figure 2, the controller 216, exemplarily implemented as a microprocessor controller, monitors Tx CDR 214A and Rx CDR 214B for a respective LOL signal on pins 606 or 608. The Tx CDR 214A and the Rx CDR 214B can generate an LOL signal using a phase locked loop ("PLL") or any other circuitry, system or device that indicates loss of lock on a signal.

[038] In addition to implementing various monitoring functionalities, the controller 216 also provides control signals to the data rate select pins 602 and 604 of Tx CDR 214A and Rx CDR 214B, respectively. In at least some implementations, the controller 216 maintains the current data rate as a default as long as there is no LOL signal transmitted on pins 606 or 608. However, in response to detecting LOL signal on pin 606 or 608, controller 216 resets the target data rate to test a new data rate. In the event that the LOL signal transmitted on pins 606 or 608 ceases, thereby indicating a correct selected data rate, controller 216 will maintain the new data rate.

[039] On the other hand, if the LOL signal transmitted on pins 606 or 608 persists, the controller 216 tests another data rate. The process of sensing the LOL signal transmitted on pins 606 or 608 and resetting the data rate continues until either an appropriate data rate has been selected or all data rates have been attempted. In one embodiment, if all data rates generate an LOL signal, the data stream 402 and/or 502, as applicable, is passed through the IC 212 without clock and data recovery.

[040] Thus, the controller 216 obviates the need for a user to set and/or select operational data rates. As a result, exemplary embodiments of the invention are well suited for use in connection with systems and devices where data rates can vary.

[041] It should be noted that in the exemplary embodiments illustrated in Figures 2 and 3 (below), the controller 216 and 708, respectively, is included as an element of the

transceiver/transponder module. More generally however, the controller may be disposed external to the module in some embodiments. Alternatively, the controller can be integrated onto the same chips as the IC. In yet other implementations, no controller is required. An example of one such implementation is considered below in connection with the discussion of Figure 4. Accordingly, the scope of the invention should not be construed to be limited to the exemplary illustrated embodiments.

III.   Aspects of Exemplary MUX/DEMUX Signal Modification Circuitry

[042] As noted earlier herein, signal modification circuitry directed to automatic implementation of data rate changes and associated functionality can be implemented in a variety of different forms. With attention now to Figure 3, a transceiver/transponder module 700 is illustrated that includes an IC 702. In this exemplary embodiment, transceiver/transponder module 700 further includes a MUX 704, DEMUX 706, both of which are configured for communication with a controller 708. Both the MUX 704 and DEMUX 706 are configured to receive various inputs and generate various outputs. It should be noted that the MUX 704 and DEMUX 706, and IC 702, and other circuitry of transceivers/transponders may be integrated on a single IC, or configured as discrete components, as suggested by the phantom line in Figure 3. In general, and as discussed in further detail below, the MUX 704 and DEMUX 706 serve to multiplex and demultiplex, respectively, data streams associated with the transceiver/transponder module 700.

[043] With more particular reference now to Figure 3, the MUX 704 is configured to receive a data input 802 from the host 300 (see Figure 1), as well as a reference clock input 804. In one exemplary implementation, the reference clock input 804 comprises a

parallel input clock or, alternatively, a Tx clock. In some implementations, MUX 704 and DEMUX 706 share the reference clock input 804, thereby reducing the amount of required circuitry on transceiver/transponder module 700. In addition to the foregoing, the MUX 704 generates a data output 806 to transmitter 208 (see Figure 1). More particularly, parallel data from host device 300 (see Figure 1) enters MUX 704 via data input 802. The MUX 704 then serializes the received data and transmits the data, as data output 806, to transmitter 208 (see Figure 1).

[044] With continuing reference to Figure 3, the DEMUX 706 receives, on the receive path 202A, an input 902 from the receiver 204 (see Figure 1). The DEMUX 706 also generates a data output 904. More particularly, serialized data enters DEMUX 706 from receiver 204 via data input 902. The MUX 706 then deserializes the received data and transmits the data, as data output 904, to transmitter 208 (see Figure 1). As discussed in further detail below, 'data rate select' pins 1002 and 1004 couple the controller 708 to MUX 704 and DEMUX 706, respectively.

[045] More particularly, the respective data rate select pins 1002 and 1004 enable automatic selection of an operational data rate. If the data rate of the input data stream 902 is out of the range of the selected data rate of MUX 704 and DEMUX 706, the MUX 704 and DEMUX 706, as applicable, generates a loss of lock ("LOL") signal on pins 1102 and/or 1104, as applicable. However, if MUX 704 or DEMUX 706 is locked, no LOL signal is generated for the respective CDR. In the exemplary arrangement illustrated in Figure 3, the controller 708, exemplarily implemented as a microprocessor controller, monitors MUX 704 and DEMUX 706 for a respective LOL signal on pins 1102 and/or 1104. The MUX 704 and DEMUX 706 can generate an LOL signal using a PLL or any other circuitry, system or device that indicates loss of lock on a signal.

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[046] In addition to implementing various monitoring functionalities, the controller 216 also provides control signals to the data rate select pins 1102 and 1104 of MUX 704 and DEMUX 706, respectively. In at least some implementations, the controller 708 maintains the current data rate as a default as long as there is no LOL signal transmitted on pins 1102 or 1104. However, in response to detecting LOL signal on pin 1102 or 1104, controller 708 resets the target data rate to test a new data rate. In the event that the LOL signal transmitted on pins 1102 or 1104 ceases, thereby indicating a correct selected data rate, controller 708 will maintain the new data rate.

[047] On the other hand, if the LOL signal transmitted on pins 1102 or 1104 persists, the controller 708 tests another data rate. The process of sensing the LOL signal transmitted on pins 1102 or 1104 and resetting the data rate continues until either an appropriate data rate has been selected or all data rates have been attempted. In one embodiment, if all data rates generate an LOL signal, the data stream 802 and/or 904, as applicable, is passed through the IC 702 without a data rate change.

[048] It should be noted that IC 702 may alternatively include a SERDES (not shown) with an automatically selectable data rate. In this alternative implementation, the SERDES is also configured to generate an LOL signal. Similar to the automatic selection of a data rate for a MUX/DEMUX implementation, the data rate of operation can be automatically selected using the LOL signal from the SERDES.

IV.   Aspects of Exemplary Controllerless CDR Signal Modification Circuitry

[049] As noted elsewhere herein, at least some implementations of the invention are effective in implementing automatic data rate adjustment functionality without

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requiring an external controller or external control signal. Directing attention now to Figure 4, details are provided concerning an example of such an implementation.

[050] In particular, a transceiver/transponder 1200 is provided that has includes an IC 1202. Among other things, the IC 1202 includes a rate selectable transmitter Tx CDR 1204A and a rate selectable receiver Rx CDR 1204B. The transmitter rate selectable Tx CDR 1204A receives a data stream from host device 300 (see Figure 1) by way of data pin 1302. The Tx CDR 1204A then transmits the data stream to transmitter 208 (see Figure 1) via data output pin 1304, or alternatively, via bypass 1305. The bypass signal is indicated at 1306. Similarly, Rx CDR 1204B receives input data via input pin 1402 and transmits the data stream to host device 300 via output pin 1404 or, alternatively, bypass 1405. The bypass signal is indicated at 1406.

[051] In the illustrated implementation, neither the rate selectable transmitter Tx CDR 1204A nor the rate selectable receiver Rx CDR 1204B is coupled to a controller or an external clock. Rather, in the illustrated embodiment, the Tx CDR 1204A and Rx CDR 1204B are configured to automatically select the proper data rate of operation without external control. More particularly, the Tx CDR 1204A and Rx CDR 1204B are configured to automatically detect an LOL 1502 and 1504, respectively, and automatically attempt various data rates of operation. If any of the selected data rates succeeds in stopping the LOL, then the Tx CDR 1204A and Rx CDR 1204B operate at the selected data rate. If LOL does not cease for any of the selected data rates, the Tx CDR 1204A and Rx CDR 1204B allows the input data stream to bypass the Tx CDR 1204A and Rx CDR 1204B.

[052] Thus, because exemplary embodiments of the transceiver/transponder module 1200 are self-contained so as to be able to implement data rate changes in environments

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where the host device does not include a clock or control input or other I/O or device for specifying data rate changes, embodiments of the invention can be implemented in systems conforming to a wide variety of different standards and protocols. As discussed below, embodiments of the CDR disclosed herein are useful in a wide variety of applications.

[053] By way of example, eliminating the need for an external clock or oscillator correspondingly eliminates the need for certain I/O capabilities. While this aspect of exemplary embodiments of the invention benefits manufacturers by reducing costs, this aspect also allows CDRs to be readily added to systems that do not support additional CDRs. For example, industry standards typically do not provide the necessary I/O for adding a CDR to an SFP or SFF type module. Specifically, adding a CDR to existing SFP or SFF type modules requires additional pin connects. Since the standard for SFP and SFF type modules has been set however, the connectors for these types of modules cannot be modified to accommodate additional pins.

[054] However, embodiments of the CDR disclosed herein can readily be added to an existing SFP or SFF type module to perform various useful functions, such as eye opening for example. In one exemplary embodiment and associated operational scenario, a 4 Gb/s Fibre Channel module is configured to run at 4, 2, or 1 Gb/s or lower. The eye opening functionality of the CDR is only used for higher data rates, such as rates of 2 Gb/s or 4 Gb/s. When the CDR detects a loss of lock signal, the CDR selects a data rate of about 4 Gb/s, and then about 2Gb/s. If the loss of lock signal persists, the CDR determines that the operational data rate is slower than 2 Gb/s and takes itself offline.

V.   Aspects of An Exemplary Data Rate Selection Method

[055]   The present invention also includes a method for automatically selecting the data rate of a transceiver/transponder. Directing attention now to Figure 5, aspects of an exemplary method 1600 for automatically selecting a data rate are indicated. At stage 1602, an input data stream having a data rate is received. The process 1600 then idles at stage 1604 unless and until an LOL signal, indicating that the data rate of the input data stream deviates from the selected data rate by a predetermined margin, is received.

[056]   Upon receipt of an LOL signal, the process 1600 then advances to stage 1606 where a predetermined range of selectable data rates $R_1...R_n$ associated with the transceiver/transponder or other device, is accessed. In two exemplary alternative embodiments, a predetermined group of two or more discrete data rates, or a single predetermined selectable data rate, is accessed.

[057]   Next, the process 1600 advances to stage 1608 where the operational data rate is set to match the first, or next, data rate, as applicable, in the range. The process 1600 then proceeds to stage 1610 where a decision point is reached. In particular, if LOL persists, as would be the case where the new data rate of the CDR does not match the data rate of the input data stream, the process 1600 returns to stage 1608 to reset the data rate of the CDR to the next data rate in the range or group of selectable data rates $R_1...R_n$.

[058]   After each reset of the data rate, the process 1600 advances to stage 1612 where a determination is made as to whether all the data rates in the range have been test. If all of the data rates have not been tested, the process then repeats until a data rate has been set that causes deassertion of LOL. After LOL has been deasserted in response to the setting of a particular data rate, the process 1600 returns to stage 1604 for LOL idle.

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[059] It may be the case in some evolutions that none of the data rates in the range will cause the deassertion of LOL. Thus, in the event that the data rate of the CDR is set to every data rate in the range without causing deassertion of LOL, the process 1600 advances to stage 1610 where 'bypass' is set. At some point subsequent to the setting of 'bypass,' the process 1600 may be reset and return to stage 1604 for LOL idle.

VI.   General Aspects of Software

[060] As disclosed elsewhere herein, aspects of implementations of the invention may be implemented by way of various computing devices and associated software. Such computing devices may comprise a special purpose or general purpose computer that includes various computer hardware, as discussed in greater detail below.

[061] When information is transferred or provided over a network or another communications connection (either hardwired, wireless, or a combination of hardwired or wireless) to a computer, the computer properly views the connection as a computer-readable medium. Thus, any such a connection is properly termed a computer-readable medium. Combinations of the above should also be included within the scope of computer-readable media. Computer-executable instructions comprise, for example, instructions and content which cause a general purpose computer, special purpose computer, or special purpose processing device to perform a certain function or group of functions.

[062] The following discussion is intended to provide a brief, general description of an exemplary computing environment in which aspects of exemplary embodiments of the invention may be implemented. Although not required, aspects of the invention may be described in the general context of computer-executable instructions, such as program

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modules, being executed by computers in network environments. Generally, program modules include routines, programs, objects, components, and content structures that perform particular tasks or implement particular abstract content types. Computer-executable instructions, associated content structures, and program modules represent examples of the program code means for executing steps of the methods disclosed herein. The particular sequence of such executable instructions or associated content structures represent examples of corresponding acts for implementing the functions described in such steps.

[063] Of course, the invention may be practiced in network computing environments with many types of computer system configurations, including personal computers, hand-held devices, multi-processor systems, microprocessor-based or programmable consumer electronics, network PCs, minicomputers, mainframe computers, and the like. The invention may also be practiced in distributed computing environments where tasks are performed by local and remote processing devices that are linked (either by hardwired links, wireless links, or by a combination of hardwired or wireless links) through a communications network. In a distributed computing environment for example, program modules may be located in both local and remote memory storage devices.

[064] The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

WORKMAN NYDEGGER
A PROFESSIONAL CORPORATION
ATTORNEYS AT LAW
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UTAH 84111